IN THE UNITED STATES PATETN AND TRADEMARK OFFICE

In re Application of:
Hung Chang LIN and Chiang-Hua YEH

Art unit: 2816

Serial No. 10/608,303

Examiner: NGUYEN, Minh T

Filed: June 30, 2003

For: AUTOMATIC WIDEBAND QUADRATURE FREQUENCY GENERATOR

AMENDMENT

Commissioner for Patents
P.O. Box. 1450
Alexandria, VA 22313-1450

Sir:

In response to USPTO communication dated April 4, 2004, please amend the application as follows:

IN THE SPECFICATION:

On page 3, line 20, delete "PMOS current mirror M3 and M4" and insert therefor --PMOS current mirror M4 and M5--; delete "M2 and M4" and insert therefore --M3 and M5--; on line 21, delete "V_{Bias}" such that the paragraph reads as follows:

--Fig. 4 shows CMOS differential pair used as an analog multiplier. The load for the differential pair is a PMOS current mirror [M3, M4] M4, M5. The output at the common drains of [M2 and M4] M3 and M5 is single- ended and is clamped to a dc voltage [V_{Bias}] through a load resistance R_L, which is ac shorted by capacitor C_L to set the ac output voltage to zero. Similar to Fig.3c, the ac voltage V_Q appearing at the gate of M2 is at quadrature phase with the ac input voltage V_I applied to the current source M1. The biasing circuit for the current source is similar to that in Fig.3c.--

IN THE CLAIMS:

Claim 1. (canceled)

Claim 2. (currently amended) [The] A quadrature frequency generator [as described in claim 1, wherein said multiplier is an], comprising:

a single-stage analog multiplier having a first input terminal, a second input terminal and an output terminal for producing an output equal to the product of the signals appearing at said first input terminal and said second input terminal;

a first ac signal applied to said first input terminal;

an ac short-circuit at the output terminal, and